REMARKS

By way of this amendment and reply to the Office Action mailed January 30, 2003, claims 1, 6, 11, 18 and 29-32 have been amended. Claims 1-4, 6-9, 11-16 and 18-32 are presently pending for further consideration.

Applicants' representative appreciates the indication in the Office Action that claims 18-23 and 28 are allowed, as well as the fact that claims 6-9, 26 and 29-32 are not rejected over any art of record.

In the Office Action, claims 29-32 were rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth on page 2 of the Office Action. Claims 29-32 have been amended to conform to the sequence of steps as described in the specification and in the drawings. For example, the planarizing step a) is shown in Figure 12A of the drawings, and the forming of the oxide film is shown in Figure 12B of the drawings, and the masking of the oxide film in the high density region is shown in Figure 13A of the drawings. Therefore, claims 29-32 are now believed to fully comply with the requirements set forth in 35 U.S.C. § 112, first paragraph.

In the Office Action, claims 6-9, 26 and 30 were rejected under 35 U.S.C. § 112, second paragraph, for the reasons set forth on page 3 of the Office Action. The Office Action asserts that Figures 18A and 18B of the drawings disclose etching the first nitride film in only the low-density region, and that the specification never discloses masking the high-density region of the semiconductor substrate. Applicants' respectfully disagree with this assertion made in the Office Action. In particular, please refer to Figure 13A of the drawings, which clearly shows the etching of the first nitride film 131 in the high density region 102 after a mask has been provided to the high density region 102. Therefore, claims 6-9, 26 and 30 fully comply with the requirements set forth in 35 U.S.C. § 112, second paragraph..

In the Office Action, claims 1-4, 25, 11-16 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,326,270 to Lee et al. This rejection, to the extent that it may be applied to the presently

pending claims 1-4, 25, 11-16 and 27, is traversed for at least the reasons given below.

The presently pending independent claims 1, 6, 11 and 18 have each been amended to include features shown best in Figure 13A of the drawings, whereby the second nitride film 202 has been removed from the portions of the first nitride film 131 (in the high density region 102) that form sidewalls for the gate electrodes 116. With such a construction, the first nitride film serves as an etching stopper, while the second nitride film serves as a barrier layer for blocking impurities from traveling from the interlayer insulating film to the substrate.

As recited in each of the presently pending independent claims 1, 6, 11 and 18, portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step. See, for example, the middle two gate electrodes 116 in the high density region 102 in Figure 13A, whereby each of their respective sidewalls have the second nitride film 202 removed therefrom. Also, the outer sidewalls for the other four gate electrodes 116 in the high density region have the second nitride film 202 removed therefrom.

Lee et al., on the other hand, utilizes a second nitride layer 119 that serves as an etching stopper, and that does not serve as a barrier layer with respect to an interlayer insulating film 120. Also, as clearly seen in Figure 5 of Lee et al., his second nitride layer 119 remains on all of the sidewalls of his gate electrodes 108, in direct contact with his first nitride layer 112a that serves as the sidewalls for the gate electrodes 108.

Therefore, since Lee et al. does not teach or suggest all of the features recited in independent claims 1, 6, 11 and 18, all of the presently pending claims are patentable over the cited art of record.

Furthermore, dependent claims 2-4, 25, 12-16 and 27 are patentable for the specific features recited in those claims. In particular, with respect to dependent claims 3 and 13, Applicant again strongly disagrees with the Office

Action's assertion about the thickness of the second nitride film being a matter of design choice. Rather, as explained on page 26, lines 3-9 of the specification, the thickness of the second nitride film is thin enough so as to pass the forming gas used in a final annealing step, so as not to impair the recovery of an interfacial layer. Also, the thickness of the second nitride film is thick enough so as to act as a barrier to prevent impurities from an interlayer insulating film from being diffused into the semiconductor substrate when the substrate is annealed in water vapor, as explained on page 25, lines 18-25 of the specification. Thus, the thickness of the second nitride film as recited in claims 3 and 13 is clearly not a matter of design choice, but rather an inventive concept that that allows the second nitride film to serve many different roles at the same time.

Therefore, for the reasons stated above, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is earnestly solicited.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

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Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Mark d-Up Claims:

1. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein [all] portions of said second nitride film that are in direct contact with said first nitride film <u>and that are</u> positioned on <u>at least one of the respective</u> sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

6. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also to expose said nitride protective films on said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein [all] portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

11. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes in said low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein [all] portions of said second nitride film that are in direct contact with said first nitride film <u>and that are</u> positioned on <u>at least one of the respective</u> sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

18. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein [all] portions of said second nitride film that are in direct contact with said first nitride film <u>and that are</u> positioned on <u>at least one of the respective</u> sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

29. (Amended) A method according to claim 1, further comprising the [steps] step of:

a) planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the [steps] step a)[, b) and c) are] is performed [in sequence between the step of forming the interlayer insulating film and] after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

30. (Amended) A method according to claim 6, further comprising the [steps] step of:

a) planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the [steps] step a)[, b) and c) are] is performed [in sequence between the step of forming the interlayer insulating film and] after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

31. (Amended) A method according to claim 11, further comprising the [steps] step of:

a) planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the [steps] step a)[, b) and c) are] is performed [in sequence between the step of forming the interlayer insulating film and] after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

32. (Amended) A method according to claim 18, further comprising the [steps] step of:

a) planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the [steps] step a)[, b) and c) are] is performed [in sequence between the step of forming the interlayer insulating film and] after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.